THE INVENTION CLAIMED IS:

1. A method of forming an integrated circuit comprising:

providing a semiconductor substrate that is doped with a set concentration of an oxidizable dopant of a type that segregates to the top surface of a silicide when the semiconductor substrate is reacted to form such a silicide;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a silicide on the source/drain junctions and segregating dopant to the top surface of the silicide;

oxidizing the dopant on the top surface of the segregated dopant to form an insulating layer of oxidized dopant above the silicide;

depositing an interlayer dielectric above the semiconductor substrate; and

forming contacts and connection points in the interlayer dielectric to the insulating layer of oxidized dopant above the silicide.

2. The method as claimed in claim 1 wherein forming contacts and connection points further comprises simultaneously forming closed connection points and open connection points.

3. The method as claimed in claim 1 further comprising:

configuring at least a portion of the insulating layer of oxidized dopant as anti-fuse programmable elements; and

forming an electrical closed circuit through at least one of the anti-fuse programmable elements.

4. The method as claimed in claim 1 wherein the semiconductor substrate is a silicon substrate that is doped with a set concentration of arsenic dopant to form an n-type semiconductor region.

5. The method as claimed in claim 1 wherein forming the contacts in the interlayer dielectric to the insulating oxide layer above the silicide uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

6. A method of forming an integrated circuit comprising:

providing a semiconductor substrate that is doped with a set concentration of an oxidizable dopant of a type that segregates to the top surface of a silicide when the semiconductor substrate is reacted to form such a silicide;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate and low and high concentration regions therein of the oxidizable dopant;

forming a silicide on the source/drain junctions and on the gate, and segregating dopant from the high concentration regions to the top surface of the silicide on the source/drain junctions;

oxidizing the dopant on the top surface of the segregated dopant on the source/drain junctions to form an insulating layer of oxidized dopant above the silicide;

depositing an interlayer dielectric above the semiconductor substrate; and

forming contacts and connection points in the interlayer dielectric to the insulating layer of oxidized dopant above the high concentration regions, and to the silicide above the low concentration regions.

7. The method as claimed in claim 6 wherein forming contacts and connection points further comprises simultaneously forming closed connection points above the low concentration regions and open connection points above the high concentration regions.

8. The method as claimed in claim 6 further comprising:

configuring at least a portion of the insulating layer of oxidized dopant as anti-fuse programmable elements; and

forming an electrical closed circuit through at least one of the anti-fuse programmable elements.

9. The method as claimed in claim 6 wherein the semiconductor substrate is a silicon substrate that is doped with a set concentration of arsenic dopant to form an n-type semiconductor region.

10. The method as claimed in claim 6 wherein forming the contacts to the insulating layer of oxidized dopant and to the silicide further comprises forming cores within a barrier metal using materials selected from a group consisting of tantalum, titanium,

tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

11. An integrated circuit comprising:

a semiconductor substrate that is doped with a set concentration of an oxidizable dopant of a type that is segregated on top of a silicide;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

a silicide on the source/drain junctions;

segregated dopant on the top surface of the silicide;

an insulating layer of oxidized dopant on the top surface of the segregated dopant above the silicide;

an interlayer dielectric above the semiconductor substrate; and

contacts and connection points in the interlayer dielectric to the insulating layer of oxidized dopant above the silicide.

12. The integrated circuit as claimed in claim 11 wherein the contacts and connection points further comprise closed connection points and open connection points.

13. The integrated circuit as claimed in claim 11 further comprising:

at least a portion of the insulating layer of oxidized dopant being configured as anti-fuse programmable elements; and

an electrical closed circuit through at least one of the anti-fuse programmable elements.

14. The integrated circuit as claimed in claim 11 wherein the semiconductor substrate is a silicon substrate that is doped with a set concentration of arsenic dopant to form an n-type semiconductor region.

15. The integrated circuit as claimed in claim 11 wherein the contacts in the interlayer dielectric to the insulating oxide layer above the silicide use materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

16. An integrated circuit comprising:

a semiconductor substrate that is doped with a set concentration of an oxidizable dopant of a type that is segregated on top of a silicide;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate and low and high concentration regions therein of the oxidizable dopant;

a silicide on the source/drain junctions and on the gate;

segregated dopant from the high concentration regions on the top surface of the silicide on the source/drain junctions;

an insulating layer of oxidized dopant on the top surface of the segregated dopant above the silicide;

an interlayer dielectric above the semiconductor substrate; and

contacts and connection points in the interlayer dielectric to the insulating layer of oxidized dopant above the high concentration regions, and to the silicide above the low concentration regions.

17. The integrated circuit as claimed in claim 16 wherein the contacts and connection points further comprise closed connection points above the low concentration regions and open connection points above the high concentration regions.

18. The integrated circuit as claimed in claim 16 further comprising:

at least a portion of the insulating layer of oxidized dopant being configured as anti-fuse programmable elements; and

an electrical closed circuit through at least one of the anti-fuse programmable elements.

19. The integrated circuit as claimed in claim 16 wherein the semiconductor substrate is a silicon substrate that is doped with a set concentration of arsenic dopant to form an n-type semiconductor region.

20. The integrated circuit as claimed in claim 16 wherein the contacts to the insulating layer of oxidized dopant and to the silicide further comprise cores within a barrier metal formed of materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.